

A

B

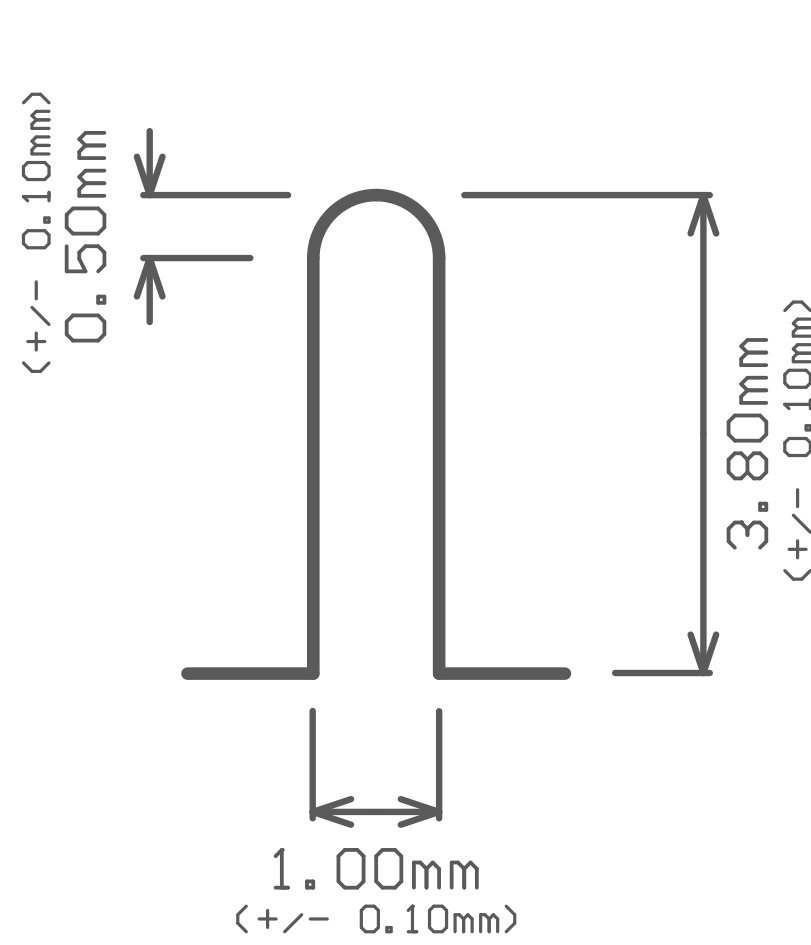
C

D

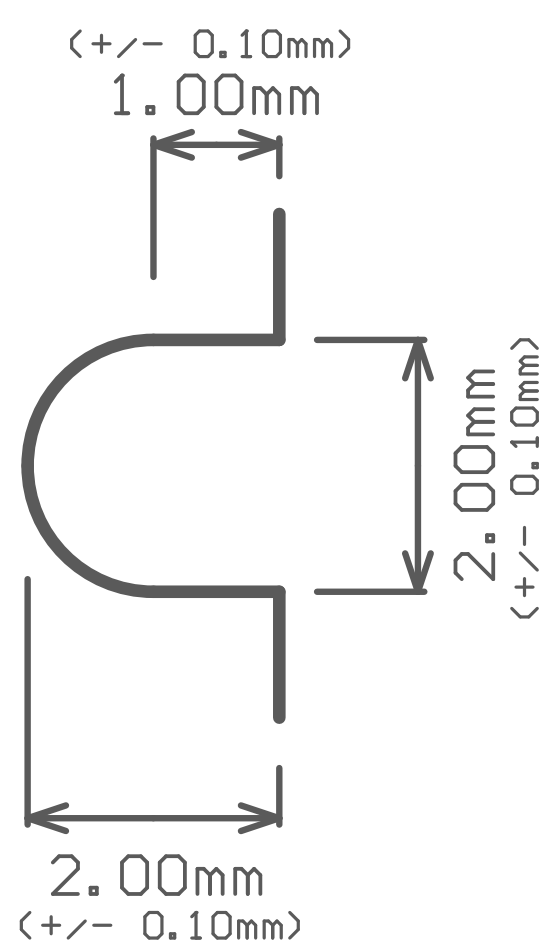
A

B

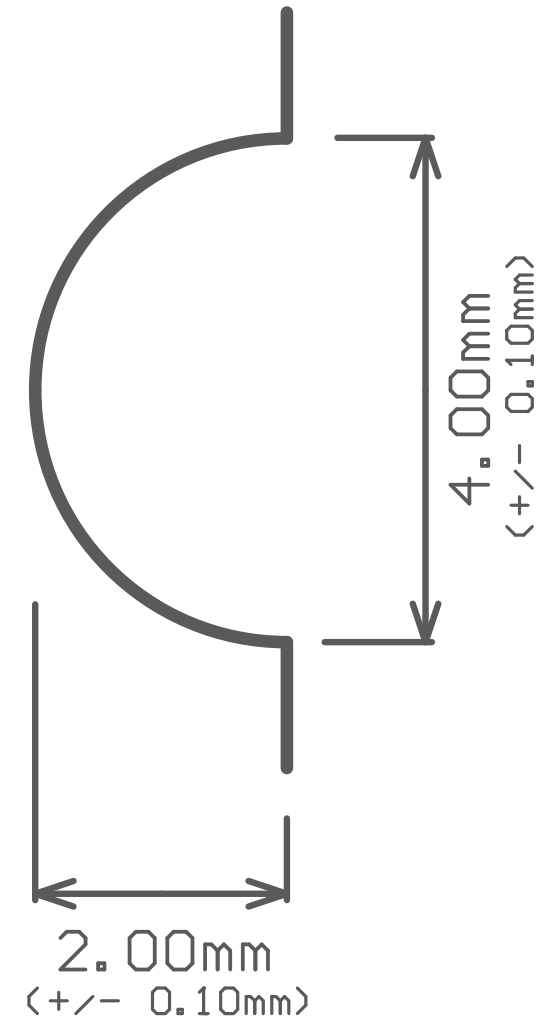
D



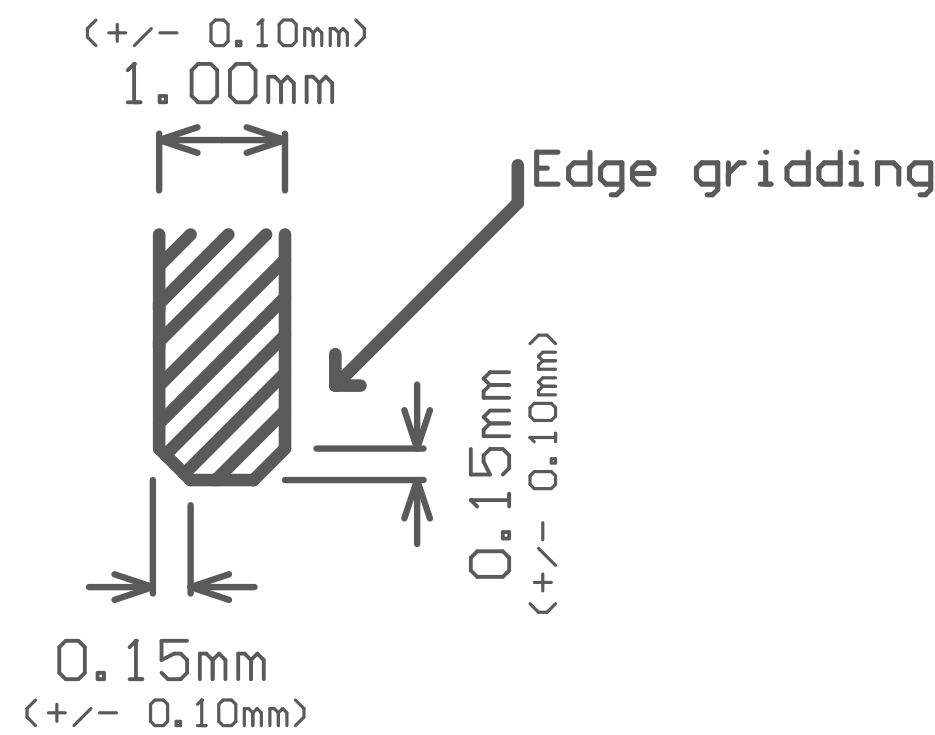
Detail 1



Detail 2

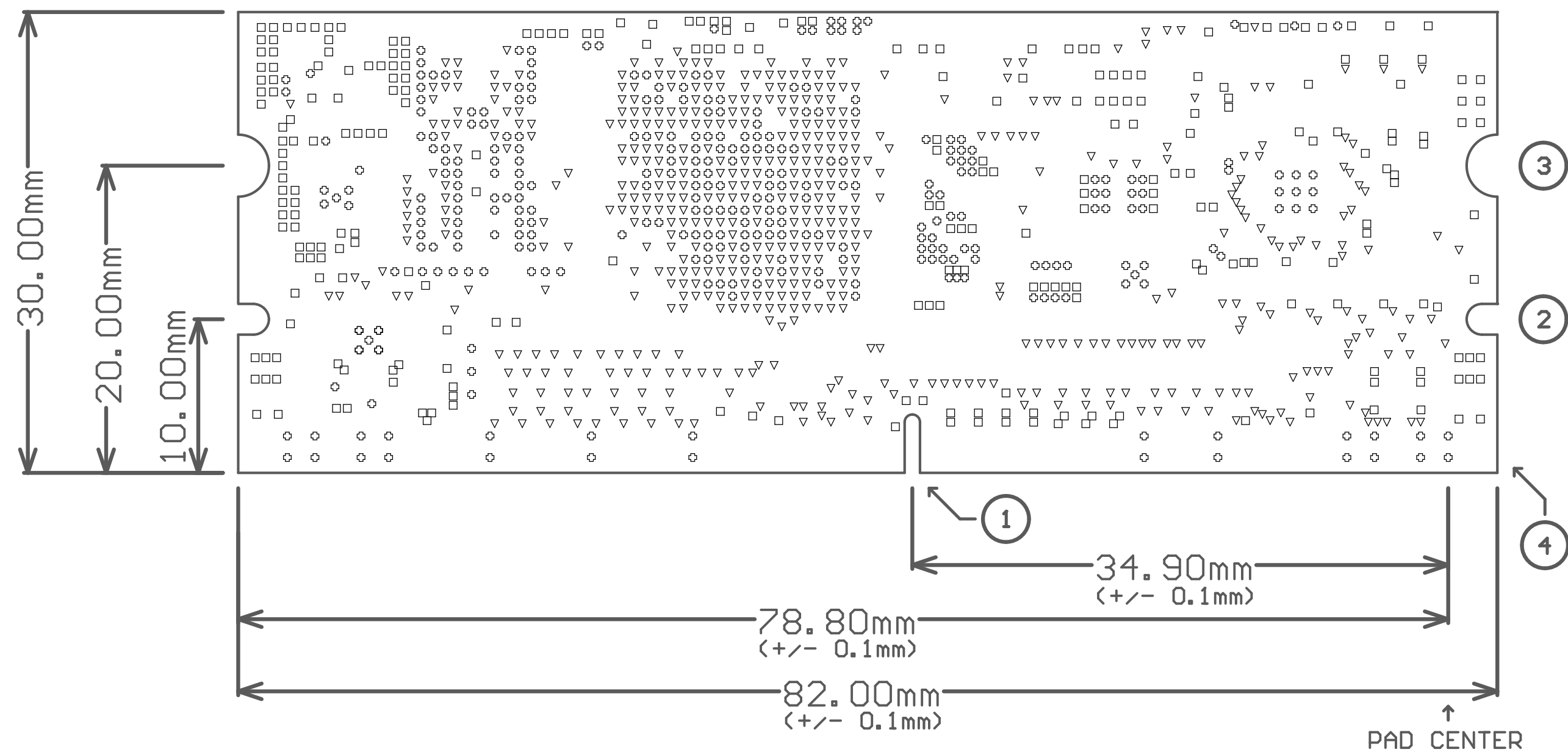


Detail 3



Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



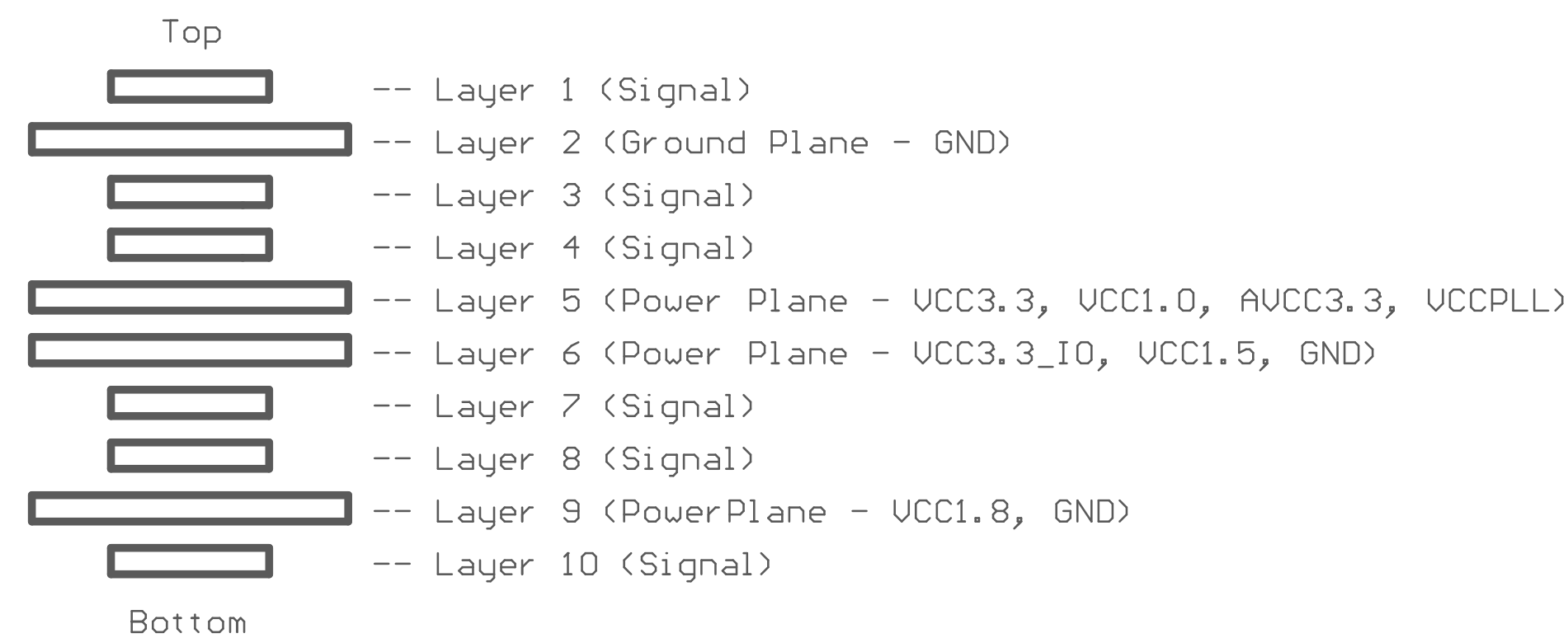
Drill Guide

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
□	268	8.00mil (0.203mm)	PTH	Round	-	-
⊕	315	7.00mil (0.178mm)	PTH	Round	-	-
▽	530	6.00mil (0.152mm)	PTH	Round	-	-
	1113 Total					

Specifications:

- Dielectric material is Tetrafunctional FR-4 with $T_g > 170\text{ }^{\circ}\text{C}$
- Overall thickness is 1.0mm $\pm 0.10\text{mm}$
- Board dimentions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
- Panelization
 - Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - Panels should contain fiducial marks for X,Y alignment
- Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
- All layers use 1/2 oz. copper (before plating)
- Holes:
 - Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - Drills are plated-through holes and their locations are given in a separate drill file.
- Finish:
 - Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - Overall board finish is immersion gold.
- Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
- Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimagable, with maximum thickness of 3 mils
- Layers 2, 5, 6 and 9 are power planes and are INVERTED
- Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
- Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
- Combination of bow and twist shall not exceed 10 mils/inch along any direction
- Design origin is at the bottom-left corner of the PCB
- Testing:
 - All layers to undergo optical inspection (machine-based) of all layers before lamination
 - Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
- Locations in IPC-D-356A file are given in 2.4 English units
- South edge-to-edge connector details:
 - Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

FILE NAME:
ZYNQ_IPMC.PCBDOC

TITLE:
ZYNQ—IPMC

PART NO.:

REV:
revB1

DWG NO.:

SCALE:
1:1